What is claimed is:

1. A method for forming an electrical insulating layer on bit lines of the flash memory, the method comprising the steps of:

providing a semiconductor substrate having a plurality of gate stacks wherein each of said gate stacks comprises a conductive layer, a mask layer and a cap layer, and a plurality of spacing are located between said gate stacks;

forming a dielectric layer on said gate stacks to fills into said spacing wherein said dielectric layer is higher than said cap layer;

forming a planarized layer on said dielectric layer to generate a planar surface;

performing a first etching step to totally remove said dielectric layer on said cap layer and simultaneously forming a spacing dielectric layer on said spacing;

performing a second etching step to remove said cap layer wherein the etching rate of said dielectric layer is less than that of said mask layer so that said spacing dielectric layer has a round top and slant sides to prevent a thin film from stress concentration; and

removing said mask layer and then remaining said spacing dielectric layer to form said electrical insulating layer.

2. The method of claim 1, wherein said conductive layer comprises a polyisilicon layer.

3. The method of claim 1, wherein said dielectric layer comprises a silicon-oxide layer.

4. The method of claim 3, wherein the step of forming said silicon-oxide layer

comprises high-density plasma chemical vapor deposition (HDPCVD).

5. The method of claim 1, wherein said planarized layer comprises a kind of organic material generated by a spin-on process.

6. The method of claim 1, after the step of said forming a planarized layer is completed, further comprising a etching step for etching said planarized layer and said dielectric layer to totally remove away said planarized layer wherein the etching rate of said planarized layer is less than that of said dielectric layer.

7. The method of claim 6, wherein said etching rate ratio between said dielectric layer and said planarized layer has a range from 1 to 10 during said etching step.

8. The method of claim 1, wherein the etching rate of said dielectric layer is larger than that of said cap layer during said first etching step.

9. The method of claim 8, wherein the etching rate ratio between said dielectric layer and said cap layer has a range from 1 to 10.

10. The method of claim 1, wherein said etching rate ratio between said dielectric layer and said mask layer has a range from 0 to 1 during said second etching step.

11. A method for forming an electrical insulating layer on bit lines of the flash

memory, the method comprising the steps of:

sequentially forming a plurality of gate stacks on the gate region of a semiconductor substrate wherein each of said gate stacks has a conductive layer, a mask layer and a cap layer, and a plurality of spacing are located between said gate stacks;

forming a dielectric layer on the semiconductor substrate to cap said gate stacks and to fill into said spacing wherein said dielectric layer is higher than said cap layer;

forming a planarized layer on said dielectric layer to generate a planar surface;

etching said planarized layer and said dielectric layer for removing totally said planarized layer wherein the etching rate of said planarized layer is less than that of said dielectric layer and simultaneously forming a spacing dielectric layer on said spacing;

removing said cap layer wherein the etching rate of said dielectric layer is less than that of said mask layer so that said spacing dielectric layer has a round top and slant sides to prevent a thin film from stress concentration; and

removing said mask layer and then remaining said spacing dielectric layer to form said electrical insulating layer.

12 The method of claim 11, wherein said conductive layer comprises a polyisilicon layer.

13. The method of claim 11, wherein said dielectric layer comprises a silicon-oxide layer.

14. The method of claim 13, wherein the step of forming said silicon-oxide

layer comprises high-density plasma chemical vapor deposition (HDPCVD).

15. The method of claim 11, wherein said planarized layer comprises a kind of organic material generated by a spin-on process.

16. The method of claim 11, wherein said etching rate ratio between said dielectric layer and said planarized layer has a range from 1 to 10 in the step of etching said planarized layer and said dielectric layer.

17. The method of claim 11, further comprising a etching step remove said dielectric on said cap layer after the step of etching said planarized layer and said dielectric layer.

18. The method of claim 17, wherein the etching rate of said dielectric layer is larger than that of said cap layer.

19. The method of claim 18, wherein the etching rate ratio between said dielectric layer and said cap layer has a range from 1 to 10.

20. The method of claim 11, wherein the etching rate ratio between said dielectric layer and said mask layer has a range from 0 to 1 during the step of removing said mask layer.